Amendments to the Drawings:

The attached sheet of drawings includes changed to Fig. 1. This sheet, which includes Fig. 1, replaces the original sheet including Fig. 1. In Figure 1, previously omitted references to N and M have been added.

Attachment: Replacement sheet

REMARKS

Claims 1-4, 6-12, and 14-24 are pending in the Application. Claims 1, 9, and 17 are independent. Claims 1, 6-7, 9, 14-15, and 17 have been amended. Claims 5 and 13 have been cancelled without prejudice.

Claim Objections

The Patent Office objected to claim 1 due to informalities. Claim 1 has been amended and is believed not objectionable.

Claim Rejections – 35 USC § 103(a)

Claims 1-5, 8-13, 16-17, and 24 were rejected under 35 U.S.C. § 103(a) as being un-patentable over Voogel (U.S. Patent No. 6,362,651) ("Voogel"), in view of Shigeki et al. (U.S. Publication No. 2001/0011345) ("Shigeki"). Applicant respectfully traverses these rejections.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. <u>First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings</u> (emphasis added). Second, there must be a reasonable expectation of success. Finally, <u>the prior art reference (or references when combined) must teach or suggest all the claim limitations.</u>" (emphasis added) (MPEP § 2143). "<u>If an independent claim is non-obvious under 35 U.S.C. 103, then any claim depending therefrom is non-obvious.</u>" (emphasis added) *In re Fine*, 837 F. 2d 1071, 5USPQ2d 1596 (Fed. Cir. 1988). Applicant respectfully submits that the claims rejected under this section include elements that have not been disclosed, taught or suggested by any of the references cited by the Patent Office, either alone or in combination.

Applicant respectfully submits that claims 1-5, 8-13, 16-17, and 24 recite elements not disclosed by Voogel or Shigeki, alone or in combination. For

example, claim 1 recites:

> cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and
>
> packaging and testing said N by M array of platform array units.

The Patent Office cites to Voogel for the above limitations (Col. 2, lines 65-67; Col. 3, lines 1-3; FIG. 4(A)). However, Voogel does not disclose cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer. Voogel discloses multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips. Voogel does not mention a platform array unit platform. Voogel discloses a single platform (300) as a single wafer (FIG. 4(A)). Voogel does not mention cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer.

Multiple field-programmable gate array circuits are not equivalent to platform array units. Therefore, multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips are not equivalent to cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer. Thus, Voogel does not disclose cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer.

Furthermore, the Patent Office cites to Shigeki for each of said plurality of platform array units including at least one core and at least one pre-manufactured processor (FIG. 1). However, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor. Shigeki discloses a CPU core design that is particularly suited to be programmed within a FPGA. A CPU core design particularly suited to be programmed within a FPGA is not equivalent to a platform array unit including at least one core and at least one pre-manufactured processor. Therefore, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and Voogel and Shigeki, alone or in combination, do not disclose the method of claim 1.

Claim 9 recites:

means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and

means for packaging and testing said N by M array of platform array units.

The Patent Office cites to Voogel for the above limitations (Col. 2, lines 65-67; Col. 3, lines 1-3; FIG. 4(A)). However, Voogel does not disclose means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer. Voogel discloses multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips. Voogel does not mention a platform array unit platform. Voogel discloses a single platform (300) as a single wafer (FIG. 4(A)). Voogel does not mention cutting N by M array of platform array units within a single platform array

unit platform from a field programmable platform array wafer.

Multiple field-programmable gate array circuits are not equivalent to platform array units. Therefore, multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips are not equivalent to means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer. Thus, Voogel does not disclose means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer.

Furthermore, the Patent Office cites to Shigeki for each of said plurality of platform array units including at least one core and at least one pre-manufactured processor (FIG. 1). However, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor. Shigeki discloses a CPU core design that is particularly suited to be programmed by a customer within a FPGA. A CPU core design particularly suited to be programmed within a FPGA is not equivalent to a platform array unit including at least one core and at least one pre-manufactured processor. Therefore, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and Voogel and Shigeki, alone or in combination, do not disclose the system of claim 9.

Claim 17 recites:
a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor;

wherein interconnect between said plurality of platform array units being pre-routed.

The Patent Office cites to Voogel for the above limitations (Col. 2, lines 65-67; Col. 3, lines 1-3; FIG. 4(A)). However, Voogel does not disclose a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer. Voogel discloses multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips. Voogel does not mention a platform array unit platform. Voogel discloses a single platform (300) as a single wafer (FIG. 4(A)). Voogel does not mention cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer.

Multiple field-programmable gate array circuits are not equivalent to platform array units. Therefore, multiple field-programmable gate array circuits in a wafer with device linking conductors where the wafer may be diced into both single field-programmable gate array chips and multiple field-programmable gate array chips are not equivalent to cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer. Thus, Voogel does not disclose cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer.

Furthermore, the Patent Office cites to Shigeki for each of said plurality of platform array units including at least one core and at least one pre-manufactured processor (FIG. 1). However, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor. Shigeki discloses a CPU core design that is particularly suited to be programmed by a customer within a FPGA. A CPU core

design particularly suited to be programmed by a customer within a FPGA is not equivalent to a platform array unit including at least one core and at least one pre-manufactured processor. Therefore, Shigeki does not disclose each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and Voogel and Shigeki, alone or in combination, do not disclose the device of claim 17.

Thus, under *In re Fine*, a *prima facie* case of obviousness has not been established for claims 1, 9, and 17. Claims 2-5, 8, 10-13, 16, and 24 are believed allowable based on their dependence upon allowable base claims.

The Patent Office rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Shigeki in further view of Mastro et al. (United States Publication No. 2002/0091977) ("Mastro"). Applicant respectfully traverses. Claim 6 depends from Claim 1, which is allowable for the reasons stated above, and is believed allowable due to its dependence upon an allowable base claim. Claim 14 depends from Claim 9, which is allowable for the reasons stated above, and is thus believed allowable due to its dependence upon an allowable base claim.

The Patent Office rejected Claims 7 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Shigeki in further view of Or-bach et al. (United States Publication No. 2001/0038297) ("Or-bach"). Applicant respectfully traverses. Claim 7 depends from Claim 1, which is allowable for the reasons stated above, and is believed allowable due to its dependence upon an allowable base claim. Claim 15 depends from Claim 9, which is allowable for the reasons stated above, and is thus believed allowable due to its dependence upon an allowable base claim.

The Patent Office rejected Claims 18 and 20-23 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Shigeki in view of Lee et al. (U.S. Patent

No. 6,222,212) ("Lee"). Applicant respectfully traverses. Claims 18 and 20-23 depend from Claim 17, which is allowable for the reasons stated above, and is thus believed allowable due to their dependence on an allowable base claim.

The Patent Office rejected Claim 19 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Shigeki in view of Huang et al. (United States Patent No. 6,396,129) ("Glen"). Applicant respectfully traverses. Claim 19 depends from Claim 17, which is allowable for the reasons stated above, and is thus believed allowable based on its dependence on an allowable base claim.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,
LSI Corporation,

Dated: October 17, 2008   By: _____

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